\*\*\* Running vivado

with args -log myand.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source myand.tcl

\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:09 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source myand.tcl -notrace

Command: synth\_design -top myand -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t-csg324'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t-csg324'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 12356

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 308.707 ; gain = 78.742

---------------------------------------------------------------------------------

INFO: [Synth 8-638] synthesizing module 'myand' [T:/myand.v/myand.v.srcs/sources\_1/new/myand.v:23]

INFO: [Synth 8-256] done synthesizing module 'myand' (1#1) [T:/myand.v/myand.v.srcs/sources\_1/new/myand.v:23]

---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 347.785 ; gain = 117.820

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 347.785 ; gain = 117.820

---------------------------------------------------------------------------------

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [T:/myand.v/myand.v.srcs/constrs\_1/new/myinv\_pin.xdc]

Finished Parsing XDC File [T:/myand.v/myand.v.srcs/constrs\_1/new/myinv\_pin.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [T:/myand.v/myand.v.srcs/constrs\_1/new/myinv\_pin.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/myand\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/myand\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 563.578 ; gain = 0.000

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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 563.578 ; gain = 333.613

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 563.578 ; gain = 333.613

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 563.578 ; gain = 333.613

---------------------------------------------------------------------------------

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 563.578 ; gain = 333.613

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

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Finished RTL Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

Hierarchical RTL Component report

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Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

---------------------------------------------------------------------------------

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

---------------------------------------------------------------------------------

Finished Part Resource Summary

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---------------------------------------------------------------------------------

Start Cross Boundary and Area Optimization

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---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 563.578 ; gain = 333.613

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Applying XDC Timing Constraints

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---------------------------------------------------------------------------------

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 618.445 ; gain = 388.480

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Start Timing Optimization

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Timing Optimization : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 618.445 ; gain = 388.480

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start IO Insertion

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---------------------------------------------------------------------------------

Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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---------------------------------------------------------------------------------

Finished Renaming Generated Instances : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Rebuilding User Hierarchy

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---------------------------------------------------------------------------------

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

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---------------------------------------------------------------------------------

Start Renaming Generated Ports

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---------------------------------------------------------------------------------

Finished Renaming Generated Ports : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |LUT2 | 1|

|2 |IBUF | 2|

|3 |OBUF | 1|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 4|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:11 ; elapsed = 00:00:14 . Memory (MB): peak = 627.586 ; gain = 181.828

Synthesis Optimization Complete : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 627.586 ; gain = 397.621

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 2 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

13 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:19 ; elapsed = 00:00:20 . Memory (MB): peak = 640.109 ; gain = 416.910

INFO: [Common 17-1381] The checkpoint 'T:/myand.v/myand.v.runs/synth\_1/myand.dcp' has been generated.

report\_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.014 . Memory (MB): peak = 640.109 ; gain = 0.000

INFO: [Common 17-206] Exiting Vivado at Wed Jan 23 16:12:29 2019...